THAT WHICH IS CLAIMED IS:

1. A phase locked loop (PLL) circuit, comprising:

a controlled oscillator circuit operative to generate an output clock signal responsive to an oscillator control signal according to a plurality of selectable transfer functions;

an oscillator control signal generator circuit that generates the oscillator control signal responsive to the output clock signal and a reference clock signal; and

a transfer function control circuit operative to transition operation of the controlled oscillator from a first one of the transfer functions to a second one of the transfer functions responsive to the oscillator control signal.

2. A PLL circuit according to Claim 1, wherein the oscillator control signal comprises an oscillator control voltage, and wherein the transfer function control circuit is operative to transition operation of the controlled oscillator circuit from the first transfer function to the second transfer function responsive to a voltage range criterion for the oscillator control voltage.

3. A PLL circuit according to Claim 2:

wherein the oscillator control signal generator circuit comprises:

a loop filter; and

a charge pump circuit operative to charge and discharge the loop filter responsive to the output clock signal and the reference clock signal to generate the oscillator control voltage;

wherein the transfer function control circuit is operative to enable and disable the charge pump circuit based on the voltage range criterion for the oscillator control voltage.

4. A PLL circuit according to Claim 3, wherein the oscillator control signal generator circuit further comprises a phase/frequency detector (PFD) circuit, and wherein the transfer function control circuit is operative to control the PFD circuit to enable and disable operation of the charge pump circuit.

5. A PLL circuit according to Claim 3, wherein the charge pump circuit comprises a first charge pump circuit, and wherein transfer function control circuit

further comprises a second charge pump circuit that controls the oscillator control voltage when the first charge pump circuit is disabled.

6. A PLL circuit according to Claim 5, wherein the transfer function control circuit is operative to disable the first charge pump based on a first voltage range criterion for the oscillator control voltage, to cause the second charge pump circuit to drive the oscillator control voltage to a voltage indicative of reduced phase/frequency error while the first charge pump is disabled, and to re-enable the first charge pump based on a second voltage range criterion for the oscillator control voltage.

7. A PLL circuit according to Claim 2, wherein the transfer function control circuit comprises:

a window comparator circuit operative to generate a limit signal indicative of a relationship between the oscillator control voltage and a voltage window; and

a transfer function selector circuit that causes the controlled oscillator to operate according to a selected transfer function responsive to the limit signal.

8. A PLL circuit according to Claim 1, wherein the transfer function control circuit is operative to step the controlled oscillator circuit through a succession of the transfer functions in response to a change in a frequency of the reference clock signal and to enable a closed loop including the oscillator control signal generator circuit and the controlled oscillator circuit upon each selection of the succession of transfer functions.

9. A PLL circuit according to Claim 8, further comprising a lock detector circuit operative to generate a lock indication signal indicative of phase agreement between the output clock signal and the reference clock signal, and wherein the transfer function control circuit is operative to initiate stepping of the controlled oscillator circuit through the succession of transfer functions responsive to the lock indication signal.

10. A PLL circuit, comprising:

a voltage-controlled oscillator (VCO) circuit that is configured to generate an output clock signal responsive to an oscillator control voltage according to a plurality of selectable transfer functions;

a loop filter coupled to an oscillator control voltage input of the VCO circuit;

a charge pump circuit coupled to the loop filter;

a PFD circuit that controls the charge pump responsive to the output clock signal and a reference clock signal; and

a transfer function control circuit operative to transition operation of the VCO circuit from a first one of the transfer functions to a second one of the transfer functions responsive to the oscillator control voltage.

11. A PLL circuit according to Claim 10, further comprising a common mode feedback (CMFB) circuit operative to receive a CMFB signal from the loop filter and to responsively control a common mode voltage of the oscillator control voltage, and wherein the transfer function control circuit is operative to transition operation of the VCO circuit from the first transfer function to the second transfer function responsive to the CMFB voltage.

12. A PLL circuit according to Claim 11, wherein the charge pump circuit comprises a first charge pump circuit, and wherein the transfer function control circuit comprises:

a second charge pump circuit operative to control the CMFB voltage;

a first window comparator circuit operative to disable the PFD circuit, to transition operation of the VCO circuit from the first transfer function to the second transfer function and to enable the second charge pump circuit responsive to excursion of the CMFB voltage outside a first voltage range; and

a second window comparator circuit operative to cause the second charge pump circuit to drive the CMFB voltage toward a second voltage range and to re-enable the PFD circuit responsive to the CMFB voltage reaching the second voltage range.

13. A PLL circuit according to Claim 12, further comprising a lock detector circuit that generates a lock indication signal indicative of a phase agreement

between the output clock signal the reference clock signal, and wherein the first window comparator circuit is operative to vary the first voltage range responsive to the lock indication signal.

14. A PLL circuit according to Claim 10, wherein the transfer function control circuit is operative to step the VCO circuit through a succession of the transfer functions in response to a change in a frequency of the reference clock signal and to enable a closed loop including the PFD circuit, the charge pump and the VCO circuit upon selection of each of the succession of transfer functions.

15. A PLL circuit according to Claim 14, further comprising a lock detector circuit operative to generate a lock indication signal indicative of phase agreement between the output clock signal and the reference clock signal, and wherein the transfer function control circuit is operative to initiate stepping of the VCO circuit through the succession of transfer functions responsive to the lock indication signal.

16. A method of operating a PLL circuit including a controlled oscillator that produces an output clock signal having a frequency that varies according to an oscillator control signal, the method comprising:

transitioning operation of the controlled oscillator from a first transfer function to a second transfer function responsive to the oscillator control signal.

17. A method according to Claim 15, wherein the oscillator control signal comprises an oscillator control voltage, and wherein transitioning operating of the controlled oscillator from a first transfer function to a second transfer function comprises transitioning operation of the controlled oscillator circuit from the first transfer function to the second transfer function responsive to a voltage range criterion for the oscillator control voltage.

18. A method according to Claim 17, wherein the PLL circuit comprises a loop filter and a charge pump circuit operative to charge and discharge the loop filter responsive to the output clock signal and the reference clock signal to generate the oscillator control voltage, and wherein transitioning operation of the controlled

oscillator circuit from the first transfer function to the second transfer function responsive to a voltage range criterion for the oscillator control voltage comprises enabling and disabling the charge pump circuit based on the voltage range criterion for the oscillator control voltage.

19. A method according to Claim 18, wherein the PLL circuit further comprises a phase/frequency detector (PFD) circuit, and wherein enabling and disabling the charge pump circuit based on the voltage range criterion for the oscillator control voltage comprises controlling the PFD circuit responsive to the voltage range criterion to enable and disable operation of the charge pump circuit.

20. A method according to Claim 18, further comprising driving the oscillator control voltage to a voltage indicative of reduced phase/frequency error while the charge pump is disabled, and then re-enabling the charge pump based on a second voltage range criterion for the oscillator control voltage.

21. A method according to Claim 16, comprising:

stepping the controlled oscillator through a succession of the transfer functions in response to a change in a frequency of the reference clock signal; and

enabling a closed loop including the controlled oscillator circuit upon selection of each of the succession of transfer functions.